

RCS file: /s6/cvsroot/euterpe/BOM,v

Working file: BOM

head: 5.105

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1940; selected revisions: 33

description:

top level BOM

-----  
revision 3.804

date: 1995/06/02 00:36:56; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/nasty

Fix hermnasty

-----  
revision 3.803

date: 1995/06/02 00:17:30; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

uu/uuprblmfrz.Veqn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would not be requested at the same time. Generally this is true, except for the one-issue window before the interrupt can cancel latent heldback store-and-swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt at the same time a SAAS heldback hiccup released, causing the event entry to be aborted leaving the hiccup to go to the SAAS but not unexpectedly with the user code running in event mode.

-----  
revision 3.802

date: 1995/06/01 00:49:51; author: fwo; state: Exp; lines: +2 -2

Release Target: euterpe/compass/layouts

stpadvdda.ly

stpadrf.ly

stpadnormal.ly

stpadlowres.ly

stpadlowcap.ly

stpadgnd.ly

stpadcorner.ly

stpadbasevss.ly

stpadbase.ly

These files should have been checked into proteus, not euterpe.

-----  
revision 3.801

date: 1995/06/01 00:34:29; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel

heldback\_debug.sig

New trace file.

-----  
revision 3.800

date: 1995/05/31 18:36:26; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

xlu  
rg  
nb  
hc0  
gf  
es  
at  
dr

-----  
revision 3.799  
date: 1995/05/31 17:53:58; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
template

var0 -> cvar0

-----  
revision 3.798  
date: 1995/05/31 17:34:22; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel/hermes

Arrrrrrgh. Trying again.

-----  
revision 3.797  
date: 1995/05/31 17:28:40; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel/hermes

Another try.

-----  
revision 3.796  
date: 1995/05/31 17:13:30; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel/hermes

New hermes tests.

-----  
revision 3.795  
date: 1995/05/31 14:08:50; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
template

exinbash\_0 rules should be euterpe

-----  
revision 3.794  
date: 1995/05/31 06:37:13; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/dr

Added this flat pim file, droutdpcontrol.pim, to  
place drprbcm and other drout control plas and  
random cells.

-----  
revision 3.793  
date: 1995/05/31 06:31:38; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cc

Two changes rolled into one:

1) logic (wiring only) change:

nbcout control field bit 14 (bit 4 of physical address) to come from hexcount lsb for both writebacks and fills, not hardwired to zero. This is for backing from hermes interleaved spaces.

2) layout change: some hexcount cells in cc\_control\_blob moved down to avoid collision at the top level.

Converges in zero iterations.

-----  
revision 3.792

date: 1995/05/31 05:18:32; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
template

Increase exintbast simtime

-----  
revision 3.791

date: 1995/05/31 03:46:46; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
template

Added exintbash variations

-----  
revision 3.790

date: 1995/05/31 02:40:32; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/doc

.0 BOM for major snapshot update

euterpe.doc revision 1.25

date: 1995/03/21 16:38:12 LT; author: rich; state: Exp; lines: +24 -15

altered the content and wording of the Sofa and Hermes clock generation descriptions to be up to date.

memory.mif revision 4.34

date: 1995/05/30 11:45:04 LT; author: bobm; state: Exp; lines: +295 -2477

Two rows in the Interleaved Hermes Channel physical address space table were mislabeled.

verify.html revision 18.15

date: 1995/05/02 11:50:37 LT; author: doi; state: Exp; lines: +5 -1

describe additional functionality for the "forward-only-active" keyword

-----  
revision 3.789

date: 1995/05/30 21:44:42; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/nasty

Fix potential bug in all nasty tests - checking final results before all cylinder finished.

Also fixed bug in cachesynchnasty2, where r6 and r8 were not saved/restored by the event handler.

-----  
revision 3.788

date: 1995/05/30 20:47:58; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/compass

.0 release for next major snapshot update

-----  
revision 3.787

date: 1995/05/30 20:43:00; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

euterpe.V hz/hz.V: Correct stage of net names to go with the fixing this in CC  
(the hz.V stage names were left alone but annotated with correcting comments;  
euterpe.V changed HZtCdNdXHzrdS1S4L7L8 to HZtCdNdXHzrdS1S4L9L10):  
cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages in  
building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot fix,  
so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1.  
euterpe.status: Delete note saying we need a tau phase check (done).  
Clarify impact of interruptibility of GGFMul on prohibiting src=dst.

-----  
revision 3.786

date: 1995/05/30 16:58:38; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Added signals and cvs string.

-----  
revision 3.785

date: 1995/05/30 13:25:12; author: vanthof; state: Exp; lines: +2 -2  
Release Target: euterpe/compass/layouts

stpadbase.ly  
stpadbasevss.ly  
stpadcorner.ly  
stpadgnd.ly  
stpadlowcap.ly  
stpadlowres.ly  
stpadnormal.ly  
stpadrf.ly  
stpadvdda.ly  
vlsi.log

updating space xformer pad cells

-----  
revision 3.784

date: 1995/05/29 20:00:09; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Debug hermnasty

-----  
revision 3.783

date: 1995/05/29 01:16:32; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

places 100% at 900ps again

-----  
revision 3.782

date: 1995/05/28 22:24:54; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/es

```

move a couple of cells to stop overlap with mc.  Latest power.tab.top
-----
revision 3.781
date: 1995/05/28 22:21:02;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

carve hole at top of rgcr for gf.  Delete explicit DISPLAY setting from Makefile
-----
revision 3.780
date: 1995/05/28 22:17:02;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gf

shift lower 7 sections left
-----
revision 3.779
date: 1995/05/28 03:35:27;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Add rules of building _var_?_0.s
-----
revision 3.778
date: 1995/05/28 03:29:49;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Release latest versions of exintbash.S(3.2) hermnasty.S(1.8)
-----
revision 3.777
date: 1995/05/28 03:27:56;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Build _0 versions of var tests
-----
revision 3.776
date: 1995/05/28 03:15:13;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                template

Add var_0 tests
-----
revision 3.775
date: 1995/05/27 21:59:16;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                template

rearrange _var again
-----
revision 3.774
date: 1995/05/27 19:33:43;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
                template

Put cachesynchnasty2_var_a_0 at the head of the runmm regression
-----
revision 3.773
date: 1995/05/27 16:41:52;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

```

remove force of power levels on cr interface to prevent dc load problems

-----  
revision 3.772

date: 1995/05/27 08:27:36; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages  
in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot  
fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1  
noticed. Also need to update hz.V and euterpe.V to show correct staging  
and not recreate confusion as we forget what happened here. But wait for  
verification to prove this is cause of failure.  
cust\_intf.wkz: Update Cache and CTag address setup and hold times to use the  
newly-stick-approved 400ps requirements rather than the more arbitrary 50%\*tick  
requirement. This reduces requirements enough to pass DTag adrs hold.

=====

RCS file: /s6/cvsroot/euterpe/compass/BOM,v

Working file: compass/BOM

head: 7.21

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 67; selected revisions: 4

description:

-----  
revision 4.1

date: 1995/06/01 00:49:27; author: fwo; state: Exp; lines: +2 -2

Release Target: euterpe/compass/layouts

stpadvdda.ly

stpadrf.ly

stpadnormal.ly

stpadlowres.ly

stpadlowcap.ly

stpadgnd.ly

stpadcorner.ly

stpadbasevss.ly

stpadbase.ly

These files should have been checked into proteus, not euterpe.

-----  
revision 4.0

date: 1995/05/30 20:47:39; author: tbr; state: Exp; lines: +1 -1

Release Target: euterpe/compass

.0 release for next major snapshot update

-----  
revision 3.9

date: 1995/05/30 20:47:31; author: tbr; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

-----  
revision 3.8

date: 1995/05/30 13:24:50; author: vanthof; state: Exp; lines: +2 -2

Release Target: euterpe/compass/layouts

stpadbase.ly

....

```
stpadbasevss.ly
stpadcorner.ly
stpadgnd.ly
stpadlowcap.ly
stpadlowres.ly
stpadnormal.ly
stpadrf.ly
stpadvdda.ly
vlsi.log
```

updating space xformer pad cells

=====

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v

Working file: compass/layouts/BOM

head: 27.3

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 79; selected revisions: 4

description:

releasebom adding BOM

-----

revision 18.1

date: 1995/06/01 00:49:14; author: fwo; state: Exp; lines: +10 -10

Release Target: euterpe/compass/layouts

```
stpadvdda.ly
stpadrf.ly
stpadnormal.ly
stpadlowres.ly
stpadlowcap.ly
stpadgnd.ly
stpadcorner.ly
stpadbasevss.ly
stpadbase.ly
```

These files should have been checked into proteus, not euterpe.

-----

revision 18.0

date: 1995/05/30 20:47:16; author: tbr; state: Exp; lines: +1 -1

Release Target: euterpe/compass

.0 release for next major snapshot update

-----

revision 17.2

date: 1995/05/30 20:47:08; author: tbr; state: Exp; lines: +7 -34

releasebom: File needs to be up-to-date to use commit -r

-----

revision 17.1

date: 1995/05/30 13:24:40; author: vanthof; state: Exp; lines: +38 -2

Release Target: euterpe/compass/layouts

```
stpadbase.ly
stpadbasevss.ly
stpadcorner.ly
stpadgnd.ly
stpadlowcap.ly
```

stpadlowres.ly  
stpadnormal.ly  
stpadrf.ly  
stpadvdda.ly  
vlsi.log

updating space xformer pad cells

=====

RCS file: /s6/cvsroot/euterpe/doc/BOM,v  
Working file: doc/BOM  
head: 22.5  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 70;      selected revisions: 2  
description:  
BOM for doc

-----

revision 20.0  
date: 1995/05/31 02:40:14; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/doc

.0 BOM for major snapshot update

euterpe.doc revision 1.25  
date: 1995/03/21 16:38:12 LT; author: rich; state: Exp; lines: +24 -15  
altered the content and wording of the Sofa and Hermes clock generation  
descriptions to be up to date.

memory.mif revision 4.34  
date: 1995/05/30 11:45:04 LT; author: bobm; state: Exp; lines: +295 -2477  
Two rows in the Interleaved Hermes Channel physical address  
space table were mislabeled.

verify.html revision 18.15  
date: 1995/05/02 11:50:37 LT; author: doi; state: Exp; lines: +5 -1  
describe additional functionality for the "forward-only-active" keyword

-----

revision 19.8  
date: 1995/05/31 02:40:07; author: tbr; state: Exp; lines: +7 -16  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v  
Working file: doc/memory.mif  
head: 4.36  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 46;      selected revisions: 1  
description:  
-----

revision 4.34

date: 1995/05/30 18:45:04; author: bobm; state: Exp; lines: +295 -2477  
Two rows in the Interleaved Hermes Channel physical address  
space table were mislabeled.

=====

RCS file: /s6/cvsroot/euterpe/doc/debug/BOM,v  
Working file: doc/debug/BOM  
head: 3.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 1  
description:  
releasebom adding BOM

-----

revision 3.0  
date: 1995/05/31 02:39:52; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/doc

.0 BOM for major snapshot update

euterpe.doc revision 1.25  
date: 1995/03/21 16:38:12 LT; author: rich; state: Exp; lines: +24 -15  
altered the content and wording of the Sofa and Hermes clock generation  
descriptions to be up to date.

memory.mif revision 4.34  
date: 1995/05/30 11:45:04 LT; author: bobm; state: Exp; lines: +295 -2477  
Two rows in the Interleaved Hermes Channel physical address  
space table were mislabeled.

verify.html revision 18.15  
date: 1995/05/02 11:50:37 LT; author: doi; state: Exp; lines: +5 -1  
describe additional functionality for the "forward-only-active" keyword

=====

RCS file: /s6/cvsroot/euterpe/verify/BOM,v  
Working file: verify/BOM  
head: 12.34  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 404; selected revisions: 18  
description:

-----

revision 4.154  
date: 1995/06/02 00:36:32; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/nasty

Fix hermnasty

-----

revision 4.153  
date: 1995/06/01 00:34:12; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel

```

        heldback_debug.sig

New trace file.
-----
revision 4.152
date: 1995/05/31 17:53:39; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

var0 -> cvar0
-----
revision 4.151
date: 1995/05/31 17:33:54; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Arrrrrrgh. Trying again.
-----
revision 4.150
date: 1995/05/31 17:28:12; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Another try.
-----
revision 4.149
date: 1995/05/31 17:13:09; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

New hermes tests.
-----
revision 4.148
date: 1995/05/31 14:08:33; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

exinbash_0 rules should be euterpe
-----
revision 4.147
date: 1995/05/31 05:18:16; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

Increase exintbast simtime
-----
revision 4.146
date: 1995/05/31 03:46:28; author: lisar; state: Exp; lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

Added exintbash variations
-----
revision 4.145
date: 1995/05/30 21:44:18; author: jeffm; state: Exp; lines: +2 -2
Release Target: euterpe/verify/nasty

Fix potential bug in all nasty tests - checking final results before
all cylinder finished.

```

Also fixed bug in cachesynchnasty2, where r6 and r8 were not saved/restored by the event handler.

-----  
revision 4.144

date: 1995/05/30 16:58:19; author: jeffm; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Added signals and cvs string.

-----  
revision 4.143

date: 1995/05/29 19:59:55; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Debug hermnasty

-----  
revision 4.142

date: 1995/05/28 03:35:14; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/nasty

Add rules of building \_var\_?\_0.s

-----  
revision 4.141

date: 1995/05/28 03:29:36; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/nasty

Release latest versions of exintbash.S(3.2) hermnasty.S(1.8)

-----  
revision 4.140

date: 1995/05/28 03:27:43; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/nasty

Build \_0 versions of var tests

-----  
revision 4.139

date: 1995/05/28 03:15:00; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
template

Add var\_0 tests

-----  
revision 4.138

date: 1995/05/27 21:59:02; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
template

rearrange \_var again

-----  
revision 4.137

date: 1995/05/27 19:33:29; author: lisar; state: Exp; lines: +2 -2

Release Target: euterpe/verify/toplevel  
template

Put cachesynchnasty2\_var\_a\_0 at the head of the runmm regression

```

RCS file: /s6/cvsroot/euterpe/verify/nasty/BOM,v
Working file: verify/nasty/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 36;    selected revisions: 10
description:
releasebom adding BOM
-----
revision 13.0
date: 1995/06/02 00:36:17;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Fix hermnasty
-----
revision 12.1
date: 1995/06/02 00:36:10;  author: jeffm;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 12.0
date: 1995/05/30 21:44:04;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Fix potential bug in all nasty tests - checking final results before
all cylinder finished.

Also fixed bug in cachesynchnasty2, where r6 and r8 were not saved/restored
by the event handler.
-----
revision 11.1
date: 1995/05/30 21:43:54;  author: jeffm;  state: Exp;  lines: +20 -10
releasebom: File needs to be up-to-date to use commit -r
-----
revision 11.0
date: 1995/05/28 03:35:06;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Add rules of building _var_?_0.s
-----
revision 10.1
date: 1995/05/28 03:34:59;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 10.0
date: 1995/05/28 03:29:27;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Release latest versions of exintbash.S(3.2) hermnasty.S(1.8)
-----
revision 9.1
date: 1995/05/28 03:29:21;  author: lisar;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 9.0

```

date: 1995/05/28 03:27:34; author: lisar; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/nasty

Build \_0 versions of var tests

-----  
revision 8.1

date: 1995/05/28 03:27:29; author: lisar; state: Exp; lines: +4 -4  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/Makefile,v

Working file: verify/nasty/Makefile

head: 1.14

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 14; selected revisions: 2

description:  
-----

revision 1.8

date: 1995/05/28 03:34:16; author: lisar; state: Exp; lines: +26 -1

Oops forgot to add the rules (can't build locally as would clobber executables I  
ned to keep  
-----

revision 1.7

date: 1995/05/28 03:26:45; author: lisar; state: Exp; lines: +26 -26

Add \_0 build of var tests  
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty.S,v

Working file: verify/nasty/cachenasty.S

head: 1.3

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 3; selected revisions: 1

description:  
-----

revision 1.2

date: 1995/05/30 21:39:23; author: jeffm; state: Exp; lines: +2 -1

Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.  
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty2.S,v

Working file: verify/nasty/cachenasty2.S

head: 1.3

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 3; selected revisions: 1

description:

-----  
revision 1.2  
date: 1995/05/30 21:39:26; author: jeffm; state: Exp; lines: +2 -1  
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.

=====  
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty3.S,v  
Working file: verify/nasty/cachenasty3.S  
head: 1.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 1  
description:

-----  
revision 1.2  
date: 1995/05/30 21:39:28; author: jeffm; state: Exp; lines: +2 -1  
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.

=====  
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty4.S,v  
Working file: verify/nasty/cachenasty4.S  
head: 1.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4; selected revisions: 1  
description:

-----  
revision 1.2  
date: 1995/05/30 21:39:30; author: jeffm; state: Exp; lines: +2 -1  
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.

=====  
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5.S,v  
Working file: verify/nasty/cachenasty5.S  
head: 1.7  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 7; selected revisions: 1  
description:

-----  
revision 1.3  
date: 1995/05/30 21:39:32; author: jeffm; state: Exp; lines: +2 -1

Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking cylinder status.

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5_var_a1_1.exe,v
Working file: verify/nasty/cachenasty5_var_a1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 11.1
date: 1995/05/28 18:20:29;  author: lisar;  state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
=====
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5_var_b1_1.exe,v
Working file: verify/nasty/cachenasty5_var_b1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 11.1
date: 1995/05/28 18:20:34;  author: lisar;  state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
=====
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5_var_c1_1.exe,v
Working file: verify/nasty/cachenasty5_var_c1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 11.1
date: 1995/05/28 18:20:38;  author: lisar;  state: Exp;
```

Just preserving tests which have slightly different timing than the current build of the tests.  
This build found 2 HW problems. Note that these tests need to be run with DRAM in configuration 0.

=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5\_var\_d1\_1.exe,v  
Working file: verify/nasty/cachenasty5\_var\_d1\_1.exe  
head: 11.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1;      selected revisions: 1  
description:  
-----  
revision 11.1  
date: 1995/05/28 18:20:42; author: lisar; state: Exp;  
Just preserving tests which have slightly different timing than the current build of the tests.  
This build found 2 HW problems. Note that these tests need to be run with DRAM in configuration 0.

=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachenasty5\_var\_e1\_1.exe,v  
Working file: verify/nasty/cachenasty5\_var\_e1\_1.exe  
head: 11.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1;      selected revisions: 1  
description:  
-----  
revision 11.1  
date: 1995/05/28 18:20:47; author: lisar; state: Exp;  
Just preserving tests which have slightly different timing than the current build of the tests.  
This build found 2 HW problems. Note that these tests need to be run with DRAM in configuration 0.

=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty.S,v  
Working file: verify/nasty/cachesynchnasty.S  
head: 1.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3;      selected revisions: 1  
description:  
-----  
revision 1.2  
date: 1995/05/30 21:39:35; author: jeffm; state: Exp; lines: +2 -1

Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking cylinder status.

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2.S,v
Working file: verify/nasty/cachesynchnasty2.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 2
description:
```

```
-----
revision 1.4
date: 1995/06/01 16:03:15; author: jeffm; state: Exp; lines: +4 -4
Oops, wasn't turning off rupts properly before calling pass.
```

```
-----
revision 1.3
date: 1995/05/30 21:39:37; author: jeffm; state: Exp; lines: +10 -2
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.
```

Fix all to actually wait until all cylinders are finished before checking cylinder status.

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2_var_a1_1.exe,v
Working file: verify/nasty/cachesynchnasty2_var_a1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
```

```
-----
revision 11.1
date: 1995/05/28 18:20:51; author: lisar; state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2_var_b1_1.exe,v
Working file: verify/nasty/cachesynchnasty2_var_b1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
```

```
revision 11.1
date: 1995/05/28 18:20:56; author: lisar; state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2_var_c1_1.exe,v
Working file: verify/nasty/cachesynchnasty2_var_c1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
```

```
revision 11.1
date: 1995/05/28 18:21:01; author: lisar; state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2_var_d1_1.exe,v
Working file: verify/nasty/cachesynchnasty2_var_d1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
```

```
revision 11.1
date: 1995/05/28 18:21:06; author: lisar; state: Exp;
Just preserving tests which have slightly different timing than the current
build of the tests.
This build found 2 HW problems. Note that these tests need to be run with DRAM
in
configuration 0.
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/nasty/cachesynchnasty2_var_e1_1.exe,v
Working file: verify/nasty/cachesynchnasty2_var_e1_1.exe
head: 11.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
```

revision 11.1  
date: 1995/05/28 18:21:10; author: lisar; state: Exp;  
Just preserving tests which have slightly different timing than the current  
build of the tests.  
This build found 2 HW problems. Note that these tests need to be run with DRAM  
in  
configuration 0.  
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/exintbash.S,v  
Working file: verify/nasty/exintbash.S  
head: 3.7  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 7; selected revisions: 1  
description:  
-----

revision 3.3  
date: 1995/05/30 21:39:39; author: jeffm; state: Exp; lines: +2 -1  
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.  
=====

RCS file: /s6/cvsroot/euterpe/verify/nasty/hermnasty.S,v  
Working file: verify/nasty/hermnasty.S  
head: 1.15  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 15; selected revisions: 2  
description:  
-----

revision 1.10  
date: 1995/06/02 00:34:36; author: jeffm; state: Exp; lines: +11 -7  
Event daemon stores were not causing blocking reads - wrong addresses used.  
-----

revision 1.9  
date: 1995/05/30 21:39:42; author: jeffm; state: Exp; lines: +2 -1  
Fix cachesynchnasty2 to save and restore r6 and r8 on event entry/exit.

Fix all to actually wait until all cylinders are finished before checking  
cylinder status.  
=====

RCS file: /s6/cvsroot/euterpe/verify/obj/system/nasty/Makefile,v  
Working file: verify/obj/system/nasty/Makefile  
head: 1.16  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 16; selected revisions: 2

```

description:
-----
revision 1.8
date: 1995/05/28 03:34:16;  author: lisar;  state: Exp;  lines: +26 -1
Oops forgot to add the rules (can't build locally as would clobber executables I
ned to keep
-----
revision 1.7
date: 1995/05/28 03:26:45;  author: lisar;  state: Exp;  lines: +26 -26
Add _0 build of var tests
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/cable_loop_perf.S,v
Working file: verify/perf/cable_loop_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/06/01 23:52:09;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/cerb_perf.S,v
Working file: verify/perf/cerb_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 1.4
date: 1995/06/01 23:50:35;  author: claseman;  state: Exp;  lines: +7 -2
normalize cycle count
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/dcache_perf.S,v
Working file: verify/perf/dcache_perf.S
head: 1.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;      selected revisions: 1
description:
-----
revision 1.5
date: 1995/06/01 23:44:50;  author: claseman;  state: Exp;  lines: +8 -8
correct GTLB config
=====

```

```

RCS file: /s6/cvsroot/euterpe/verify/perf/dcachemiss_perf.S,v
Working file: verify/perf/dcachemiss_perf.S
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 1.3
date: 1995/06/01 23:44:54;  author: claseman;  state: Exp;  lines: +6 -6
correct GTLB config
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/dram_perf.S,v
Working file: verify/perf/dram_perf.S
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 1.4
date: 1995/06/01 23:50:10;  author: claseman;  state: Exp;  lines: +10 -2
normalize cycle count
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/eaddi_perf.S,v
Working file: verify/perf/eaddi_perf.S
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/06/01 23:52:11;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/easum_perf.S,v
Working file: verify/perf/easum_perf.S
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/06/01 23:52:12;  author: claseman;  state: Exp;

```

initial revision

```
=====
RCS file: /s6/cvsroot/euterpe/verify/perf/eshufflei4mux_perf.S,v
Working file: verify/perf/eshufflei4mux_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
```

```
-----
revision 1.1
date: 1995/06/01 23:52:14;  author: claseman;  state: Exp;
initial revision
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gextractil28_perf.S,v
Working file: verify/perf/gextractil28_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
```

```
-----
revision 1.1
date: 1995/06/01 23:52:16;  author: claseman;  state: Exp;
initial revision
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gextracti64_perf.S,v
Working file: verify/perf/gextracti64_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
```

```
-----
revision 1.1
date: 1995/06/01 23:52:18;  author: claseman;  state: Exp;
initial revision
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/ggfmul8_perf.S,v
Working file: verify/perf/ggfmul8_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
```

```
-----  
revision 1.1  
date: 1995/06/01 23:52:20;  author: claseman;  state: Exp;  
initial revision  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd16_perf.S,v  
Working file: verify/perf/gmuladd16_perf.S  
head: 1.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3;      selected revisions: 1  
description:  
-----
```

```
revision 1.1  
date: 1995/06/01 23:52:23;  author: claseman;  state: Exp;  
initial revision  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd32_perf.S,v  
Working file: verify/perf/gmuladd32_perf.S  
head: 1.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3;      selected revisions: 1  
description:  
-----
```

```
revision 1.1  
date: 1995/06/01 23:52:24;  author: claseman;  state: Exp;  
initial revision  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd64_perf.S,v  
Working file: verify/perf/gmuladd64_perf.S  
head: 1.4  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 4;      selected revisions: 1  
description:  
-----
```

```
revision 1.1  
date: 1995/06/01 23:52:27;  author: claseman;  state: Exp;  
initial revision  
=====
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd8_perf.S,v  
Working file: verify/perf/gmuladd8_perf.S  
head: 1.3  
branch:  
locks: strict  
access list:
```

```

keyword substitution: kv
total revisions: 3;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/06/01 23:52:29;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/hermes_perf.S,v
Working file: verify/perf/hermes_perf.S
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;      selected revisions: 1
description:
-----
revision 1.4
date: 1995/06/01 23:50:33;  author: claseman;  state: Exp;  lines: +9 -3
normalize cycle count
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/icachemiss_perf.S,v
Working file: verify/perf/icachemiss_perf.S
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;     selected revisions: 1
description:
-----
revision 1.1
date: 1995/06/01 23:52:31;  author: claseman;  state: Exp;
initial revision
=====

RCS file: /s6/cvsroot/euterpe/verify/perf/rom_perf.S,v
Working file: verify/perf/rom_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;      selected revisions: 1
description:
-----
revision 1.4
date: 1995/06/01 23:50:12;  author: claseman;  state: Exp;  lines: +10 -2
normalize cycle count
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1

```

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 13
description:
releasebom adding BOM
-----
revision 39.18
date: 1995/06/01 00:34:03;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/toplevel
        heldback_debug.sig

New trace file.
-----
revision 39.17
date: 1995/05/31 17:53:29;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

var0 -> cvar0
-----
revision 39.16
date: 1995/05/31 17:33:41;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Arrrrrrgh. Trying again.
-----
revision 39.15
date: 1995/05/31 17:28:00;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Another try.
-----
revision 39.14
date: 1995/05/31 17:12:57;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/toplevel/hermes

New hermes tests.
-----
revision 39.13
date: 1995/05/31 14:08:22;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

exinbash_0 rules should be euterpe
-----
revision 39.12
date: 1995/05/31 05:18:03;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
        template

Increase exintbast simtime
-----
revision 39.11
date: 1995/05/31 03:46:17;  author: lisar;  state: Exp;  lines: +2 -2

```

Release Target: euterpe/verify/toplevel  
template

Added exintbash variations

-----  
revision 39.10  
date: 1995/05/30 16:58:08; author: jeffm; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Added signals and cvs string.

-----  
revision 39.9  
date: 1995/05/29 19:59:46; author: lisar; state: Exp; lines: +5 -1  
Release Target: euterpe/verify/toplevel  
nb\_debug.srl

Debug hermnasty

-----  
revision 39.8  
date: 1995/05/28 03:14:51; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
template

Add var\_0 tests

-----  
revision 39.7  
date: 1995/05/27 21:58:53; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
template

rearrange \_var again

-----  
revision 39.6  
date: 1995/05/27 19:33:19; author: lisar; state: Exp; lines: +2 -2  
Release Target: euterpe/verify/toplevel  
template

Put cachesynchnasty2\_var\_a\_0 at the head of the runmm regression

=====  
RCS file: /s6/cvsroot/euterpe/verify/toplevel/heldback\_debug.sig,v  
Working file: verify/toplevel/heldback\_debug.sig  
head: 39.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:

-----  
revision 39.1  
date: 1995/06/01 00:30:55; author: jeffm; state: Exp;  
Trace signals to debug the synch op holdback logic.

=====  
RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermeseasy\_I1M0.S,v

```

Working file: verify/toplevel/hermeseasy_I1M0.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 1
description:
-----
revision 35.2
date: 1995/05/30 18:59:05;  author: lisar;  state: Exp;  lines: +5 -5
Avoid event register
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/nb_debug.srl,v
Working file: verify/toplevel/nb_debug.srl
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;      selected revisions: 2
description:
-----
revision 39.2
date: 1995/05/30 16:57:35;  author: jeffm;  state: Exp;  lines: +66 -2
Added signals.
-----
revision 39.1
date: 1995/05/29 19:59:30;  author: lisar;  state: Exp;
Debug hermnasty
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;     selected revisions: 7
description:
-----
revision 1.102
date: 1995/05/31 17:53:09;  author: lisar;  state: Exp;  lines: +34 -34
var0 -> cvar0
-----
revision 1.101
date: 1995/05/31 14:08:02;  author: lisar;  state: Exp;  lines: +6 -6
exinbash_0 rules should be euterpe
-----
revision 1.100
date: 1995/05/31 05:17:35;  author: lisar;  state: Exp;  lines: +12 -12
Increase exintbast simtime
-----
revision 1.99
date: 1995/05/31 03:45:46;  author: lisar;  state: Exp;  lines: +13 -1

```

Added exintbash variations

-----  
revision 1.98  
date: 1995/05/28 03:14:35; author: lisar; state: Exp; lines: +25 -11  
Add var\_0 tests

-----  
revision 1.97  
date: 1995/05/27 21:58:33; author: lisar; state: Exp; lines: +7 -8  
rearrange \_var again

-----  
revision 1.96  
date: 1995/05/27 19:32:58; author: lisar; state: Exp; lines: +10 -8  
Put cachesynchnasty2\_var\_a\_0 at the head of the runmm regression

=====  
RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/.checkoutrc,v  
Working file: verify/toplevel/hermes/.checkoutrc  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:

-----  
revision 1.1  
date: 1995/05/31 17:10:09; author: jeffm; state: Exp;  
Initial checkin.

=====  
RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/.cvsignore,v  
Working file: verify/toplevel/hermes/.cvsignore  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1; selected revisions: 1  
description:

-----  
revision 1.1  
date: 1995/05/31 17:09:16; author: jeffm; state: Exp;  
Hermes test. Test uncached and cached data and instruction access for all  
hermes spaces.

=====  
RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/BOM,v  
Working file: verify/toplevel/hermes/BOM  
head: 12.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 22; selected revisions: 6  
description:  
releasebom adding BOM

revision 4.0  
date: 1995/05/31 17:33:26; author: jeffm; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/toplevel/hermes

Arrrrrrgh. Trying again.

-----  
revision 3.1  
date: 1995/05/31 17:33:16; author: jeffm; state: Exp; lines: +2 -1  
releasebom: File needs to be up-to-date to use commit -r  
-----

revision 3.0  
date: 1995/05/31 17:27:41; author: jeffm; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/toplevel/hermes

Another try.

-----  
revision 2.1  
date: 1995/05/31 17:27:32; author: jeffm; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r  
-----

revision 2.0  
date: 1995/05/31 17:12:45; author: jeffm; state: Exp; lines: +1 -1  
Release Target: euterpe/verify/toplevel/hermes

New hermes tests.

-----  
revision 1.1  
date: 1995/05/31 17:12:37; author: jeffm; state: Exp;  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/Makefile,v  
Working file: verify/toplevel/hermes/Makefile  
head: 1.3  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 3; selected revisions: 2  
description:  
-----

revision 1.2  
date: 1995/05/31 17:21:37; author: jeffm; state: Exp; lines: +21 -21  
Minor touchup.  
-----

revision 1.1  
date: 1995/05/31 17:09:18; author: jeffm; state: Exp;  
Hermes test. Test uncached and cached data and instruction access for all  
hermes spaces.  
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/clean-request,v  
Working file: verify/toplevel/hermes/clean-request  
head: 3.1  
branch:  
locks: strict

```

access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 3.1
date: 1995/05/31 17:31:44;  author: jeffm;  state: Exp;
Missed this one.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.S,v
Working file: verify/toplevel/hermes/hermestest.S
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/31 17:09:21;  author: jeffm;  state: Exp;
Hermes test. Test uncached and cached data and instruction access for all
hermes spaces.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.ctd,v
Working file: verify/toplevel/hermes/hermestest.ctd
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/31 17:09:22;  author: jeffm;  state: Exp;
Hermes test. Test uncached and cached data and instruction access for all
hermes spaces.
=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.cti,v
Working file: verify/toplevel/hermes/hermestest.cti
head: 1.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
-----
revision 1.1
date: 1995/05/31 17:09:24;  author: jeffm;  state: Exp;
Hermes test. Test uncached and cached data and instruction access for all
hermes spaces.
=====

```

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.gmat,v  
Working file: verify/toplevel/hermes/hermestest.gmat  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1;       selected revisions: 1  
description:

-----  
revision 1.1  
date: 1995/05/31 17:09:25; author: jeffm; state: Exp;  
Hermes test. Test uncached and cached data and instruction access for all  
hermes spaces.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.gmsk,v  
Working file: verify/toplevel/hermes/hermestest.gmsk  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1;       selected revisions: 1  
description:

-----  
revision 1.1  
date: 1995/05/31 17:09:27; author: jeffm; state: Exp;  
Hermes test. Test uncached and cached data and instruction access for all  
hermes spaces.

=====

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.gxor,v  
Working file: verify/toplevel/hermes/hermestest.gxor  
head: 1.1  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 1;       selected revisions: 1  
description:

-----  
revision 1.1  
date: 1995/05/31 17:09:29; author: jeffm; state: Exp;  
Hermes test. Test uncached and cached data and instruction access for all  
hermes spaces.

=====

RCS file: /s6/cvsroot/euterpe/verify/ukernel/Makefile,v  
Working file: verify/ukernel/Makefile  
head: 1.13  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 13;     selected revisions: 3

description:

-----

revision 1.13

date: 1995/06/01 01:57:34; author: doi; state: Exp; lines: +2 -2  
whoops, used receiveMessage instead of test\_receiveMessage

-----  
revision 1.12

date: 1995/06/01 01:52:57; author: doi; state: Exp; lines: +5 -2  
add receiveMessage and test\_sendMsg to default test list (I have not got them to work with hwterp yet)

-----  
revision 1.11

date: 1995/06/01 01:46:09; author: doi; state: Exp; lines: +21 -3  
allow tests to be found in 4 different locations (ukernel/tests{,perf,stress}  
and lib/util/tests

=====

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v

Working file: verilog/BOM

head: 6.9

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1390; selected revisions: 11

description:

top level verilog BOM

-----  
revision 3.614

date: 1995/06/02 00:17:14; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

uu/uuprblmfrz.Vegn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would not be requested at the same time. Generally this is true, except for the one-issue window before the interrupt can cancel latent heldback store-and-swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt at the same time a SAAS heldback hiccup released, causing the event entry to be aborted leaving the hiccup to go to the SAAS but not unexpectedly with the user code running in event mode.

-----  
revision 3.613

date: 1995/05/31 18:35:54; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

xlu

rg

nb

hc0

gf

es

at

dr

-----  
revision 3.612

date: 1995/05/31 06:36:50; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/dr

Added this flat pim file, droutdpcontrol.pim, to  
place drprbcm and other drout control plas and  
random cells.

-----  
revision 3.611

date: 1995/05/31 06:31:18; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cc

Two changes rolled into one:

1) logic (wiring only) change:

nbcout control field bit 14 (bit 4 of physical address) to come  
from hexcount lsb for both writebacks and fills, not hardwired to zero.  
This is for backing from hermes interleaved spaces.

2) layout change: some hexcount cells in cc\_control\_blob moved  
down to avoid collision at the top level.

Converges in zero iterations.

-----  
revision 3.610

date: 1995/05/30 20:42:45; author: mws; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

euterpe.V hz/hz.V: Correct stage of net names to go with the fixing this in CC  
(the hz.V stage names were left alone but annotated with correcting comments;  
euterpe.V changed HZtCdNdxHzrdS1S4L7L8 to HZtCdNdxHzrdS1S4L9L10):

cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages in  
building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot fix,  
so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1.

euterpe.status: Delete note saying we need a tau phase check (done).  
Clarify impact of interruptibility of GGFMul on prohibiting src=dst.

-----  
revision 3.609

date: 1995/05/29 01:16:06; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc

places 100% at 900ps again

-----  
revision 3.608

date: 1995/05/28 22:24:34; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/es

move a couple of cells to stop overlap with mc. Latest power.tab.top

-----  
revision 3.607

date: 1995/05/28 22:20:40; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/rg

carve hole at top of rgcr for gf. Delete explicit DISPLAY setting from Makefile

-----  
revision 3.606

date: 1995/05/28 22:16:45; author: tbr; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/gf

shift lower 7 sections left

-----  
revision 3.605

date: 1995/05/27 16:41:36; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/rg

remove force of power levels on cr interface to prevent dc load problems

-----  
revision 3.604

date: 1995/05/27 08:27:20; author: mws; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages

in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1 noticed. Also need to update hz.V and euterpe.V to show correct staging and not recreate confusion as we forget what happened here. But wait for verification to prove this is cause of failure.

cust\_intf.wkz: Update Cache and CTag address setup and hold times to use the newly-stick-approved 400ps requirements rather than the more arbitrary 50%\*tick requirement. This reduces requirements enough to pass DTag adrs hold.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v

Working file: verilog/bsrc/BOM

head: 346.6

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 1737; selected revisions: 16

description:

-----  
revision 315.0

date: 1995/06/02 00:16:54; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu/uuprblmfrz.Vegn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would not be requested at the same time. Generally this is true, except for the one-issue window before the interrupt can cancel latent heldback store-and-swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt at the same time a SAAS heldback hiccup released, causing the event entry to be aborted leaving the hiccup to go to the SAAS but not unexpectedly with the user code running in event mode.

-----  
revision 314.1

date: 1995/06/02 00:16:41; author: mws; state: Exp; lines: +2 -2

releasebom: File needs to be up-to-date to use commit -r

-----  
revision 314.0

date: 1995/05/31 18:34:57; author: tbr; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

xlu  
rg  
nb  
hc0  
gf  
es  
at  
dr

-----  
revision 313.3

date: 1995/05/31 18:34:27; author: tbr; state: Exp; lines: +12 -9  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 313.2

date: 1995/05/31 06:36:32; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/dr

Added this flat pim file, droutdpcontrol.pim, to  
place drprbcm and other drout control plas and  
random cells.

-----  
revision 313.1

date: 1995/05/31 06:30:59; author: billz; state: Exp; lines: +2 -2  
Release Target: euterpe/verilog/bsrc/cc

Two changes rolled into one:

- 1) logic (wiring only) change:  
nbcout control field bit 14 (bit 4 of physical address) to come  
from hexcount lsb for both writebacks and fills, not hardwired to zero.  
This is for backing from hermes interleaved spaces.
- 2) layout change: some hexcount cells in cc\_control\_blob moved  
down to avoid collision at the top level.

Converges in zero iterations.

-----  
revision 313.0

date: 1995/05/30 20:42:19; author: mws; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

euterpe.V hz/hz.V: Correct stage of net names to go with the fixing this in CC  
(the hz.V stage names were left alone but annotated with correcting comments;  
euterpe.V changed HZtCdNdxHzrdS1S4L7L8 to HZtCdNdxHzrdS1S4L9L10):  
cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages in  
building hz2or4ahdr7R8, actually delivering it in R9R10. Hz.V cannot fix,  
so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1.  
euterpe.status: Delete note saying we need a tau phase check (done).  
Clarify impact of interruptibility of GGFMul on prohibiting src=dst.

-----  
revision 312.1

date: 1995/05/30 20:42:06; author: mws; state: Exp; lines: +4 -4  
releasebom: File needs to be up-to-date to use commit -r

-----  
revision 312.0

date: 1995/05/29 01:15:37; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

places 100% at 900ps again

-----

revision 311.5

date: 1995/05/29 01:15:17; author: tbr; state: Exp; lines: +6 -7

releasebom: File needs to be up-to-date to use commit -r

-----

revision 311.4

date: 1995/05/28 22:24:14; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/es

move a couple of cells to stop overlap with mc. Latest power.tab.top

-----

revision 311.3

date: 1995/05/28 22:20:19; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/rg

carve hole at top of rgcr for gf. Delete explicit DISPLAY setting from Makefile

-----

revision 311.2

date: 1995/05/28 22:16:28; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/gf

shift lower 7 sections left

-----

revision 311.1

date: 1995/05/27 16:41:20; author: tbr; state: Exp; lines: +2 -2

Release Target: euterpe/verilog/bsrc/rg

remove force of power levels on cr interface to prevent dc load problems

-----

revision 311.0

date: 1995/05/27 08:27:01; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1 noticed. Also need to update hz.V and euterpe.V to show correct staging and not recreate confusion as we forget what happened here. But wait for verification to prove this is cause of failure.

cust\_intf.wkz: Update Cache and CTag address setup and hold times to use the newly-stick-approved 400ps requirements rather than the more arbitrary 50%\*tick requirement. This reduces requirements enough to pass DTag adrs hold.

-----

revision 310.2

date: 1995/05/27 08:26:48; author: mws; state: Exp; lines: +3 -3

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v

Working file: verilog/bsrc/Makefile.tst

head: 40.104

branch:

locks: strict

access list:

keyword substitution: kv

```

total revisions: 104;    selected revisions: 1
description:
-----
revision 40.82
date: 1995/05/27 17:57:22;  author: tbr;  state: Exp;  lines: +6 -6
Make %.power.tab.top rule :: so it does not trigger a new top level iteration
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
-----
revision 312.1
date: 1995/05/30 03:07:44;  author: tbr;  state: Exp;
initial checkin
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
-----
revision 307.3
date: 1995/05/29 00:57:42;  author: tbr;  state: Exp;  lines: +67952 -67954
update from latest run
-----
revision 307.2
date: 1995/05/27 18:02:47;  author: tbr;  state: Exp;  lines: +33831 -33831
update from latest top level run
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
-----
revision 312.1
date: 1995/05/30 03:09:56;  author: tbr;  state: Exp;
initial checkin
=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip\_euterpe-base.strength,v  
Working file: verilog/bsrc/chip\_euterpe-base.strength  
head: 312.20  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 20;      selected revisions: 1  
description:

-----  
revision 312.1  
date: 1995/05/30 03:09:17;    author: tbr;    state: Exp;  
initial checkin  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip\_euterpe-base.xrf,v  
Working file: verilog/bsrc/chip\_euterpe-base.xrf  
head: 307.11  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 11;      selected revisions: 2  
description:

-----  
revision 307.3  
date: 1995/05/29 01:01:08;    author: tbr;    state: Exp;    lines: +25192 -25187  
update from latest run  
-----

revision 307.2  
date: 1995/05/27 18:00:24;    author: tbr;    state: Exp;    lines: +25381 -25234  
update from latest top level run  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v  
Working file: verilog/bsrc/euterpe.V  
head: 6.431  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 431;      selected revisions: 1  
description:

-----  
revision 6.421  
date: 1995/05/30 20:34:12;    author: mws;    state: Exp;    lines: +18 -17  
euterpe.V hz/hz.V:    Correct stage of net names to go with the fixing this in CC  
                  (the hz.V stage names were left alone but annotated with correcting comments;  
                  euterpe.V changed HZtCdNdxHzrdS1S4L7L8 to HZtCdNdxHzrdS1S4L9L10):  
cc/cc.V cc/cc\_control\_blob.pim:    Hz.V lost track of the pipeline stages in  
                  building hz2or4ahdR7R8, actually delivering it in R9R10.    Hz.V cannot fix,  
                  so we just pipeline 2 less to compensate.    Test cachesynchnasty2\_var\_a\_1.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v  
Working file: verilog/bsrc/euterpe.status  
head: 24.83

```

branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 2
description:
-----
revision 24.74
date: 1995/05/30 20:53:08;  author: mws;  state: Exp;  lines: +1 -1
Last checkin missed making ggfmul all uppercase in opcode table to
denote that it is not fully compliant.
-----
revision 24.73
date: 1995/05/30 20:35:10;  author: mws;  state: Exp;  lines: +5 -8
Delete note saying we need a tau phase check (done).
  Clarify impact of interruptibility of GGFMul on prohibiting src=dst.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_wrap.tb
head: 187.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
-----
revision 187.11
date: 1995/05/28 03:16:23;  author: lisar;  state: Exp;  lines: +2 -2
Drive Z onto pok0 (not sure why Z is better than U as at time 0 it is driven
by stimulus file - but it works!).
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;    selected revisions: 2
description:
releasebom adding BOM
-----
revision 90.0
date: 1995/05/31 18:20:26;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in
  xlu
  rg
  nb
  hc0

```

```

gf
es
at
dr
-----
revision 89.1
date: 1995/05/31 18:20:17; author: tbr; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.pim,v
Working file: verilog/bsrc/at/at.pim
head: 51.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23; selected revisions: 1
description:
-----

revision 51.22
date: 1995/05/31 05:16:16; author: tbr; state: Exp; lines: +2 -2
placement adjust for second iteration
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182; selected revisions: 4
description:
releasebom adding BOM
-----

revision 88.0
date: 1995/05/31 06:30:40; author: billz; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

Two changes rolled into one:
1) logic (wiring only) change:
nbcout control field bit 14 (bit 4 of physical address) to come
from hexcount lsb for both writebacks and fills, not hardwired to zero.
This is for backing from hermes interleaved spaces.
2) layout change: some hexcount cells in cc_control_blob moved
down to avoid collision at the top level.

Converges in zero iterations.
-----

revision 87.1
date: 1995/05/31 06:30:34; author: billz; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----

revision 87.0
date: 1995/05/27 08:22:01; author: mws; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

```
cc/cc.V cc/cc_control_blob.pim: Hz.V lost track of the pipeline stages
  in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot
  fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2_var_a_1
  noticed. Also need to update hz.V and euterpe.V to show correct staging
  and not recreate confusion as we forget what happened here. But wait for
  verification to prove this is cause of failure.
cust_intf.wkz: Update Cache and CTag address setup and hold times to use the
  newly-stick-approved 400ps requirements rather than the more abitrary 50%*tick
  requirement. This reduces requirements enough to pass DTag adrs hold.
```

```
-----
revision 86.1
date: 1995/05/27 08:21:55; author: mws; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
Working file: verilog/bsrc/cc/cc.V
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87; selected revisions: 2
description:
-----
```

```
revision 1.84
date: 1995/05/31 06:29:35; author: billz; state: Exp; lines: +10 -9
Two changes rolled into one:
1) logic (wiring only) change:
nbcout control field bit 14 (bit 4 of physical address) to come
from hexcount lsb for both writebacks and fills, not hardwired to zero.
This is for backing from hermes interleaved spaces.
2) layout change: some hexcount cells in cc_control_blob moved
down to avoid collision at the top level.
```

```
-----
revision 1.83
date: 1995/05/27 08:19:55; author: mws; state: Exp; lines: +12 -5
cc/cc.V cc/cc_control_blob.pim: Hz.V lost track of the pipeline stages
  in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot
  fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2_var_a_1
  noticed. Also need to update hz.V and euterpe.V to show correct staging
  and not recreate confusion as we forget what happened here. But wait for
  verification to prove this is cause of failure.
```

```
-----
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc_control_blob.pim,v
Working file: verilog/bsrc/cc/cc_control_blob.pim
head: 77.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8; selected revisions: 2
description:
-----
```

```
revision 77.5
```

date: 1995/05/31 06:29:37; author: billz; state: Exp; lines: +82 -84  
Two changes rolled into one:

1) logic (wiring only) change:

nbcout control field bit 14 (bit 4 of physical address) to come  
from hexcount lsb for both writebacks and fills, not hardwired to zero.  
This is for backing from hermes interleaved spaces.

2) layout change: some hexcount cells in cc\_control\_blob moved  
down to avoid collision at the top level.

-----  
revision 77.4

date: 1995/05/27 08:19:58; author: mws; state: Exp; lines: +3 -3

cc/cc.V cc/cc\_control\_blob.pim: Hz.V lost track of the pipeline stages  
in building hz2or4ahdR7R8, actually delivering it in R9R10. Hz.V cannot  
fix, so we just pipeline 2 less to compensate. Test cachesynchnasty2\_var\_a\_1  
noticed. Also need to update hz.V and euterpe.V to show correct staging  
and not recreate confusion as we forget what happened here. But wait for  
verification to prove this is cause of failure.

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v

Working file: verilog/bsrc/dr/BOM

head: 77.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 155; selected revisions: 2

description:

releasebom adding BOM

-----  
revision 73.0

date: 1995/05/31 06:36:14; author: billz; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc/dr

Added this flat pim file, droutdpcontrol.pim, to  
place drprbcsn and other drout control plas and  
random cells.

-----  
revision 72.1

date: 1995/05/31 06:36:07; author: billz; state: Exp; lines: +4 -3

releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/Makefile,v

Working file: verilog/bsrc/dr/Makefile

head: 1.34

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 34; selected revisions: 1

description:

-----  
revision 1.33

date: 1995/05/31 06:34:18; author: billz; state: Exp; lines: +2 -2

Added this flat pim file, droutdpcontrol.pim, to  
place drprbcsn and other drout control plas and

random cells.

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/droudpcontrol.pim,v
Working file: verilog/bsrc/dr/droudpcontrol.pim
head: 72.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;      selected revisions: 1
description:
```

```
-----
revision 72.1
date: 1995/05/31 06:34:19; author: billz; state: Exp;
Added this flat pim file, droudpcontrol.pim, to
place drprbcm and other droudp control plas and
random cells.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/pimlib.pl,v
Working file: verilog/bsrc/dr/pimlib.pl
head: 20.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;     selected revisions: 1
description:
```

```
-----
revision 20.16
date: 1995/05/31 06:34:21; author: billz; state: Exp; lines: +14 -16
Added this flat pim file, droudpcontrol.pim, to
place drprbcm and other droudp control plas and
random cells.
```

```
=====
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;    selected revisions: 4
description:
```

```
-----
revision 94.0
date: 1995/05/31 18:24:04; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in  
    xlu  
    rg

```

nb
hc0
gf
es
at
dr
-----
revision 93.1
date: 1995/05/31 18:23:54; author: tbr; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 93.0
date: 1995/05/28 22:23:51; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

move a couple of cells to stop overlap with mc. Latest power.tab.top
-----
revision 92.1
date: 1995/05/28 22:23:42; author: tbr; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v
Working file: verilog/bsrc/es/es.pim
head: 5.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55; selected revisions: 2
description:
-----
revision 5.53
date: 1995/05/31 05:18:01; author: tbr; state: Exp; lines: +40 -40
placement adjust for second iteration
-----
revision 5.52
date: 1995/05/28 22:22:30; author: tbr; state: Exp; lines: +82 -82
move a couple of cells to stop overlap with mc. Latest power.tab.top
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.power.tab.top,v
Working file: verilog/bsrc/es/es.power.tab.top
head: 65.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12; selected revisions: 1
description:
-----
revision 65.12
date: 1995/05/28 22:22:54; author: tbr; state: Exp; lines: +766 -766
move a couple of cells to stop overlap with mc. Latest power.tab.top
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/BOM,v

```

```

Working file: verilog/bsrc/gf/BOM
head: 37.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;    selected revisions: 4
description:
releasebom adding BOM
-----
revision 37.0
date: 1995/05/31 18:24:41;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

```

    xlu
    rg
    nb
    hc0
    gf
    es
    at
    dr

```

```

-----
revision 36.1
date: 1995/05/31 18:24:31;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 36.0
date: 1995/05/28 22:16:10;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gf

```

shift lower 7 sections left

```

-----
revision 35.1
date: 1995/05/28 22:16:04;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gf/gf.pim,v

Working file: verilog/bsrc/gf/gf.pim

head: 4.15

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 15; selected revisions: 2

description:

```

-----
revision 4.15
date: 1995/05/31 05:19:39;  author: tbr;  state: Exp;  lines: +2 -2
placement adjust for second iteration
-----

```

revision 4.14

date: 1995/05/28 22:14:58; author: tbr; state: Exp; lines: +7 -7  
shift lower 7 sections left

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v  
Working file: verilog/bsrc/hc/BOM  
head: 125.0  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 250; selected revisions: 2  
description:  
releasebom adding BOM

-----

revision 109.0  
date: 1995/05/31 18:25:30; author: tbr; state: Exp; lines: +1 -1  
Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

- xlu
- rg
- nb
- hc0
- gf
- es
- at
- dr

-----

revision 108.1  
date: 1995/05/31 18:25:21; author: tbr; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0\_control.pim,v  
Working file: verilog/bsrc/hc/hc0\_control.pim  
head: 73.25  
branch:  
locks: strict  
access list:  
keyword substitution: kv  
total revisions: 25; selected revisions: 1  
description:

-----

revision 73.16  
date: 1995/05/31 05:21:07; author: tbr; state: Exp; lines: +5 -5  
placement adjust for second iteration

=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/BOM,v  
Working file: verilog/bsrc/hz/BOM  
head: 30.0  
branch:  
locks: strict

```

access list:
keyword substitution: kv
total revisions: 58;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 30.0
date: 1995/05/30 20:39:15;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V hz/hz.V:  Correct stage of net names to go with the fixing this in CC
(the hz.V stage names were left alone but annotated with correcting comments;
euterpe.V changed HZtCdNdxHzrdS1S4L7L8 to HZtCdNdxHzrdS1S4L9L10):
cc/cc.V cc/cc_control_blob.pim:  Hz.V lost track of the pipeline stages in
building hz2or4ahdR7R8, actually delivering it in R9R10.  Hz.V cannot fix,
so we just pipeline 2 less to compensate.  Test cachesynchnasty2_var_a_1.
euterpe.status:  Delete note saying we need a tau phase check (done).
Clarify impact of interruptibility of GGFMul on prohibiting src=dst.
-----
revision 29.1
date: 1995/05/30 20:39:08;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hz/hz.V,v
Working file: verilog/bsrc/hz/hz.V
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;      selected revisions: 1
description:
-----
revision 1.15
date: 1995/05/30 20:34:51;  author: mws;  state: Exp;  lines: +81 -51
euterpe.V hz/hz.V:  Correct stage of net names to go with the fixing this in CC
(the hz.V stage names were left alone but annotated with correcting comments;
euterpe.V changed HZtCdNdxHzrdS1S4L7L8 to HZtCdNdxHzrdS1S4L9L10):
cc/cc.V cc/cc_control_blob.pim:  Hz.V lost track of the pipeline stages in
building hz2or4ahdR7R8, actually delivering it in R9R10.  Hz.V cannot fix,
so we just pipeline 2 less to compensate.  Test cachesynchnasty2_var_a_1.
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v
Working file: verilog/bsrc/nb/BOM
head: 130.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 261;      selected revisions: 2
description:
releasebom adding BOM
-----
revision 128.0
date: 1995/05/31 18:28:06;  author: tbr;  state: Exp;  lines: +1 -1

```

Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

xlu  
rg  
nb  
hc0  
gf  
es  
at  
dr

-----  
revision 127.1

date: 1995/05/31 18:27:53; author: tbr; state: Exp; lines: +2 -2  
releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb\_mid.pim,v

Working file: verilog/bsrc/nb/nb\_mid.pim

head: 88.16

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 16; selected revisions: 1

description:  
-----

revision 88.16

date: 1995/05/31 05:22:54; author: tbr; state: Exp; lines: +3 -3

placement update for second iteration  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v

Working file: verilog/bsrc/rg/BOM

head: 136.0

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 297; selected revisions: 6

description:  
-----

revision 131.0

date: 1995/05/31 18:29:09; author: tbr; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

Consolidate most recent cc bug fix to .0 BOM

Pick up placement tweaks for iteration in

xlu  
rg  
nb  
hc0

```

gf
es
at
dr
-----
revision 130.1
date: 1995/05/31 18:28:58; author: tbr; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
-----
revision 130.0
date: 1995/05/28 22:19:57; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

carve hole at top of rgcr for gf. Delete explicit DISPLAY setting from Makefile
-----
revision 129.1
date: 1995/05/28 22:19:48; author: tbr; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
-----
revision 129.0
date: 1995/05/27 16:41:03; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

remove force of power levels on cr interface to prevent dc load problems
-----
revision 128.1
date: 1995/05/27 16:40:56; author: tbr; state: Exp; lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/Makefile,v
Working file: verilog/bsrc/rg/Makefile
head: 1.50
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50; selected revisions: 1
description:
-----
revision 1.50
date: 1995/05/28 22:18:20; author: tbr; state: Exp; lines: +1 -3
carve hole at top of rgcr for gf. Delete explicit DISPLAY setting from Makefile
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/genptab.pl,v
Working file: verilog/bsrc/rg/genptab.pl
head: 82.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4; selected revisions: 1
description:
-----
revision 82.4
date: 1995/05/27 16:40:18; author: tbr; state: Exp; lines: +38 -32

```

remove force of power levels on cr interface to prevent dc load problems

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v

Working file: verilog/bsrc/rg/rg.pim

head: 82.31

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 31; selected revisions: 2

description:

-----  
revision 82.26

date: 1995/05/31 05:32:55; author: tbr; state: Exp; lines: +18 -18

placement update for second iteration

-----  
revision 82.25

date: 1995/05/28 22:18:23; author: tbr; state: Exp; lines: +8 -8

carve hole at top of rgcr for gf. Delete explicit DISPLAY setting from Makefile

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.power.tab.top,v

Working file: verilog/bsrc/rg/rg.power.tab.top

head: 79.12

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 12; selected revisions: 1

description:

-----  
revision 79.12

date: 1995/05/27 16:40:25; author: tbr; state: Exp; lines: +816 -816

remove force of power levels on cr interface to prevent dc load problems

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v

Working file: verilog/bsrc/uu/BOM

head: 218.1

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 480; selected revisions: 2

description:

-----  
revision 202.0

date: 1995/06/02 00:15:43; author: mws; state: Exp; lines: +1 -1

Release Target: euterpe/verilog/bsrc

uu/uuprblmfrz.Veqn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would not be requested at the same time. Generally this is true, except for the one-issue window before the interrupt can cancel latent heldback store-and-swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt at the same time a SAAS heldback hiccup released, causing the event entry

to be aborted leaving the hiccup to go to the SAAS but not unexpectedly  
with the user code running in event mode.

-----  
revision 201.1

date: 1995/06/02 00:15:34; author: mws; state: Exp; lines: +4 -4

releasebom: File needs to be up-to-date to use commit -r  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/Makefile,v

Working file: verilog/bsrc/uu/Makefile

head: 1.79

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 79; selected revisions: 1

description:  
-----

revision 1.79

date: 1995/06/02 00:06:50; author: mws; state: Exp; lines: +14 -2

uu/uuprblmfrz.Veqn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would  
not be requested at the same time. Generally this is true, except for the  
one-issue window before the interrupt can cancel latent heldback store-and-  
swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt  
at the same time a SAAS heldback hiccup released, causing the event entry  
to be aborted leaving the hiccup to go to the SAAS but not unexpectedly  
with the user code running in event mode.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu\_control.pim,v

Working file: verilog/bsrc/uu/uu\_control.pim

head: 68.60

branch:

locks: strict

access list:

keyword substitution: kv

total revisions: 60; selected revisions: 1

description:  
-----

revision 68.55

date: 1995/06/02 00:07:18; author: mws; state: Exp; lines: +9 -6

uu/uuprblmfrz.Veqn uu/Makefile uu/uu\_control.pim:

Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would  
not be requested at the same time. Generally this is true, except for the  
one-issue window before the interrupt can cancel latent heldback store-and-  
swap hiccups. Test cachesynchnasty2\_var\_c\_1 happened to accept an interrupt  
at the same time a SAAS heldback hiccup released, causing the event entry  
to be aborted leaving the hiccup to go to the SAAS but not unexpectedly  
with the user code running in event mode.  
=====

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmfrz.Veqn,v

Working file: verilog/bsrc/uu/uuprblmfrz.Veqn

head: 36.18

branch:

locks: strict

```

access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
-----
revision 36.17
date: 1995/06/02 00:07:43; author: mws; state: Exp; lines: +25 -4
uu/uuprblmfrz.Veqn uu/Makefile uu/uu_control.pim:
  Freeze pla at end of evblm pipe assumed that both hiccup and interrupt would
  not be requested at the same time. Generally this is true, except for the
  one-issue window before the interrupt can cancel latent heldback store-and-
  swap hiccups. Test cachesynchnasty2_var_c_1 happened to accept an interrupt
  at the same time a SAAS heldback hiccup released, causing the event entry
  to be aborted leaving the hiccup to go to the SAAS but not unexpectedly
  with the user code running in event mode.
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/BOM,v
Working file: verilog/bsrc/xlu/BOM
head: 65.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;    selected revisions: 2
description:
releasebom adding BOM
-----

```

```

revision 61.0
date: 1995/05/31 18:31:00; author: tbr; state: Exp; lines: +1 -1
Release Target: euterpe/verilog/bsrc

```

Consolidate most recent cc bug fix to .0 BOM

```

Pick up placement tweaks for iteration in
    xlu
    rg
    nb
    hc0
    gf
    es
    at
    dr
-----

```

```

revision 60.1
date: 1995/05/31 18:30:49; author: tbr; state: Exp; lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=====

```

```

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/x123.pim,v
Working file: verilog/bsrc/xlu/x123.pim
head: 33.9
branch:
locks: strict
access list:
keyword substitution: kv

```

total revisions: 9;      selected revisions: 1  
description:

-----

revision 33.9

date: 1995/05/31 05:33:54; author: tbr; state: Exp; lines: +3 -3

placement tweak for second iteration

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